

AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1024] with the following amended paragraph:

[1024] The above sequences of operations implementing the DCAS operation are executed atomically using support suitable to the particular realization. For example, in various realizations, through hardware support (e.g., as implemented by the Motorola 68040 microprocessor or as described in M. Herlihy and J. Moss, *Transactional memory: Architectural Support For Lock-Free Data Structures*, Technical Report CRL 92/07, Digital Equipment Corporation, Cambridge Research Lab, 1992, 12 pages), through non-blocking software emulation (such as described in G. Barnes, *A Method For Implementing Lock-Free Shared Data Structures*, in *Proceedings of the 5th ACM Symposium on Parallel Algorithms and Architectures*, pages 261–270, June 1993 or in N. Shavit and D. Touitou, *Software transactional memory*, *Distributed Computing*, 10(2):99–116, February 1997), or via a blocking software emulation (such as described in U.S. Patent No. 6,223,335 ~~U.S. Patent Application No. XX/xxx,xxx~~, entitled “PLATFORM INDEPENDENT DOUBLE COMPARE AND SWAP OPERATION,” naming Cartwright and Agesen as inventors, and filed December 9, 1998)..